



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :

H01L 23/02, 23/12

A1

(11) International Publication Number:

WO 94/22168

(43) International Publication Date: 29 September 1994 (29.09.94)

(21) International Application Number: PCT/US94/02113

(22) International Filing Date: 28 February 1994 (28.02.94)

(30) Priority Data:

033,596

19 March 1993 (19.03.93)

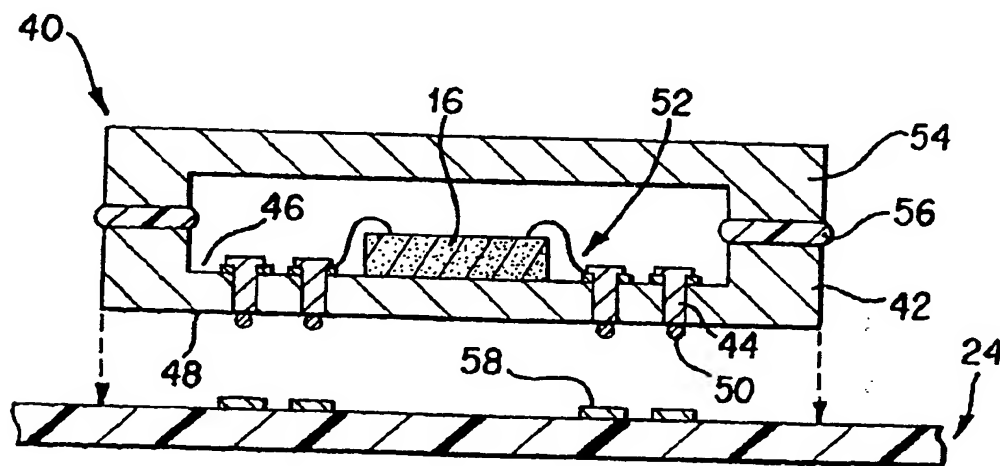
US

(71) Applicant: OLIN CORPORATION [US/US]; P.O. Box 586,
350 Knotter Drive, Cheshire, CT 06410-0586 (US).(72) Inventors: MAHULIKAR, Deepak; 20 Martleshamheath Lane,
Madison, CT 06443 (US). HOFFMAN, Paul, R.; 5542
American Avenue, Modesto, CA 95346 (US). BRADEN,
Jeffrey, S.; 1059 Alison Circle, Livermore, CA 94550 (US).(74) Agents: ROSENBLATT, Gregory, S. et al.; Wiggin & Dana,
One Century Tower, New Haven, CT 06508-1832 (US).(81) Designated States: AU, BB, BG, BR, BY, CA, CN, CZ, FI,
HU, JP, KP, KR, KZ, LK, MG, MN, MW, NO, NZ, PL,
RO, RU, SD, SK, UA, VN, European patent (AT, BE, CH,
DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE),
OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR,
NE, SN, TD, TG).

Published

With international search report.

(54) Title: BALL GRID ARRAY ELECTRONIC PACKAGE



(57) Abstract

There is provided a ball grid array package (40) for housing semiconductor devices (16). The package (40) has a metallic base (42) with conductive vias (44) extending through holes formed in the base (42). The conductive vias (44) terminate adjacent an exterior surface (48) of the base (42). A dielectric coating on at least part of the base (42) and through hole walls electrically isolates the metallic base (42) from the package circuitry (52).

BEST AVAILABLE COPY

BEST AVAILABLE COPY

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgyzstan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LJ	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LU	Luxembourg	TD	Chad
CS	Czechoslovakia	LV	Latvia	TG	Togo
CZ	Czech Republic	MC	Monaco	TJ	Tajikistan
DE	Germany	MD	Republic of Moldova	TT	Trinidad and Tobago
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America
FI	Finland	MN	Mongolia	UZ	Uzbekistan
FR	France			VN	Viet Nam
GA	Gabon				

BALL GRID ARRAY ELECTRONIC PACKAGE

The invention relates to an electronic package for housing one or more semiconductor devices. More particularly, the invention relates to a surface mount electronic package having a metallic substrate.

Microelectronic devices are typically manufactured from a semiconductor material such as silicon, germanium or gallium/arsenide. The semiconductor material is fashioned into a die, a generally rectangular structure having circuitry formed on one surface. Along the periphery of that surface are input/output pads to facilitate electrical interconnection to external components.

The semiconductor device is brittle and requires protection from moisture and mechanical damage. This protection is provided by an electronic package. The electronic package further contains an electrically conductive means to transport electrical signals between the semiconductor device and external circuitry.

One package design which minimizes space requirements and provides a high density of interconnections between the electronic device and external circuitry is the pin grid array package. One pin grid array package has a multi-layer ceramic substrate with conductive circuitry disposed between the layers. The circuitry terminates at conductive pads to which terminal pins are brazed. U.S. Patent No. 4,821,151 to Pryor et al illustrates a ceramic pin grid array package.

Molded plastic pin grid array packages are disclosed in U.S. Patent No. 4,816,426 to Bridges et al. A circuit tape has terminal pins electrically interconnected to circuit traces formed on the tape.

The assembly is partially encapsulated within a polymer resin.

Metal pin grid array packages are disclosed in U.S. Patent No. 5,098,864 to Mahulikar. An array of
5 holes is formed through a metallic substrate. Terminal pins pass through the substrate and are electrically isolated from it by a polymer resin. When the metallic substrate is aluminum based, further electrical isolation is by an anodization
10 layer on the surfaces of the substrate.

Pin grid array packages are electrically interconnected to a printed circuit board by insertion of the terminal pins through a matching array of holes formed in a printed circuit board.
15 The holes in the printed circuit board are metallized and electrical interconnection is made within the through holes of the printed circuit board.

Another type of package having a high density of
20 interconnections is a surface mount package. In a surface mount package, the printed circuit board does not require an array of holes. The leads of the package are soldered to bond pads on the printed circuit board. Typically, the leads are either bent
25 under the package in a J-shape or are bent in a gull wing shape and soldered to interconnect pads aligned with the perimeter of the package. This package is disclosed in U.S. Patent Nos. 4,706,811 to Jung et al and 5,065,281 to Hernandez et al. The solder to
30 join the electronic package to the printed circuit board is screened onto the bond pads and may contain fillers such as plated copper spheres to space the package from the board as disclosed in U.S. Patent No. 4,771,159 to O'Leary.

An advantage of a surface mount package is reduced space requirement on a printed circuit board compared to packages with leads extending from the package body. The inter-connection between the surface mount package and a printed circuit board is solder pads located on the surface of the board rather than holes drilled through to board. The number of leads in a typical leaded surface mount package is, however, limited by the peripheral area of the surface mount package.

A limitation with a pin grid array package is the array of holes formed in the printed circuit board must be aligned with the array of terminal pins extending from the package base.

Preferred packages are land grid array packages (electrical interconnection is through metallized pads on the package base) and ball grid array packages (electrical interconnection is through solder bumps formed on the base of the package). The ball grid array package does not require terminal pins and has direct solder bonds between metallized pads on a ceramic base and matching pads on a printed circuit board. Ceramic bases are a relatively poor thermal conductor as are epoxy based laminated printed circuit board bases. Metallic bases would provide an improved land grid array package. However, a means to prevent the solder joints from electrically shorting to the metallic substrate is required. Also, a means to transmit electrical signals from a printed circuit board to an encased electronic device is required.

Applicants have developed a ball grid array package having a metallic substrate which solves these problems.

Accordingly, it is an object of the invention to provide a ball grid array electronic package having a metallic base. It is the feature of the invention that the metallic base contains a plurality of
5 electrically conductive vias which, in most embodiments, are electrically isolated from the base. One end of the vias is electrically connected to external circuitry while the other end is electrically connected to an integrated circuit
10 device.

Among the advantages of the present invention are the package does not require through holes formed in a system printed circuit board. The package has a finer pitch than a pin grid array
15 package. The ball grid array package requires less peripheral space than a peripherally leaded electronic package. The package has lower lead to lead mutual inductance than leaded packages or leaded surface mount packages as well as lower lead
20 self inductance. The metallic substrate provides enhanced thermal dissipation.

In accordance with the invention, there is provided an electronic package. The electronic package has a metallic base which contains interior
25 and exterior surfaces. A plurality of electrically conductive vias extend through the metallic base with one end terminating approximately at the exterior surface. A first electrically conductive means is bonded to each of the electrically
30 conductive vias adjacent the exterior surface. A second electrically conductive means interconnects the electrically conductive vias to an electronic device mounted on the metallic base. A cover is

Figure 1 shows in cross-sectional representation a pin grid array package 10 as known from the prior art. The package has a multi-layer ceramic base 12 containing internal metallizations 14 for communicating electrical signals from external circuitry to an encapsulated integrated circuit device 16. One end of the internal metallization 14 terminates within the pin grid array package 10 and is electrically interconnected to the integrated circuit device by means of wire bond 18. The opposing end of the internal metallization 14 terminates at an exterior surface 20 of the pin grid array package 10. Terminal pins 22 are electrically interconnected to the internal metallization 14 at the exterior surface 20 such as by soldering. The external circuitry with which the integrated circuit device 16 communicates is generally disposed about a printed circuit board 24, referred to as the system board.

The system board 24 has a substrate 26 formed from a rigid or semi-rigid material such as a glass-filled epoxy. A uniform array of holes 28 having a configuration matching the array of terminal pins 22 of the pin grid array package 10 is formed through the substrate. The surfaces of the holes 28 are metallized. Metallized bond pads 32 may be included on the system board 24 and soldered to the terminal pins 22 to improve the integrity of the bond between the pin grid array package 10 and system board 24.

Figure 2 illustrates in cross-sectional representation a ball grid array package 40 in accordance with the present invention which eliminates the need for machining an array of holes in the system board. Since terminal pin to system

bonded to the metallic base with the electronic device disposed therebetween.

The above stated objects, features and advantages will become more apparent from the specification and drawings which follow.

Figure 1 shows in cross-sectional representation a pin grid array package as known from the prior art.

Figure 2 shows in cross-sectional representation a ball grid array package in accordance with an embodiment of the present invention.

Figure 3 shows in cross-sectional representation a metallic base utilized in the ball grid array package of the present invention.

Figures 4-9 illustrate in cross-sectional representation the formation of electrically conductive vias to transmit electrical signals from an encased integrated circuit device to external circuitry.

Figure 10 shows in top planar view means for electrically interconnecting conductive vias to an integrated circuit device.

Figures 11-14 show in cross-sectional representation means for electrically interconnecting conductive vias and circuitry within the ball grid array package.

Figure 15 shows in cross-sectional representation a means for utilizing the metallic bases as a ground plane.

Figure 16 shows in cross-sectional representation a cavity down ball grid array package having a metallic base and metallic cover.

Figure 17 shows in cross-sectional representation a cavity down ball grid array package having a metallic base and molded resin cover.

board hole alignment is not required, the ball grid array package can be designed with a finer pitch than the pin grid array package. Pitch is the center to center spacing between terminal pins of a pin grid array or bond pads of a ball grid array. The pitch of a pin grid array is on the order of 2.5mm (100 mils) while the land grid array is capable of 1.25mm (50 mils) or finer pitch. A further limitation on the pitch of a pin grid array package is the terminal pins must have a large enough diameter to resist bending during insertion.

The ball grid array package does not require external leads. The absence of parallel running external leads reduces mutual lead inductance and lead self inductance, both problems with "gull wing" or "J-wing" surface mount packages as well as with pin grid array packages.

The ball grid array package 40 has a metallic base 42 formed from any material having good thermal conductivity. Preferred metals include copper, aluminum and alloys thereof. Most preferred are aluminum alloys capable of forming an electrically insulating anodization layer.

Electrically conductive vias 44 extend from an interior surface 46 to an exterior surface 48 of the metallic base 42. Unlike a pin grid array package, one end of the electrically conductive via terminates approximately at exterior surface 48. A first electrically conductive means 50, such as a low melting temperature solder or an electrically conductive adhesive or sealing glass, is bonded to the electrically conductive vias 44 adjacent to the exterior surface 48. A second electrically conductive means 52, such as a combination of internal circuitry and bond wires, electrically

interconnects the electrically conductive vias 44 to an electronic device 16 mounted on the interior surface 46 of the metallic base 42.

5 The ball grid array package 40 is completed by bonding a cover 54 to the metallic base 42 with the electronic device 16 disposed therebetween. The cover 54 may be any suitable material, metal, ceramic or plastic. Preferably, the coefficient of thermal expansion of the cover 54 is approximately
10 equal to the coefficient of thermal expansion of the metallic base 42 to prevent bending of the ball grid array package 40 due to thermal expansion mismatch. The bond 56 between the metallic base 42 and cover 54 may be any suitable material such as a polymer,
15 ceramic or metallic solder. Polymer adhesives, such as thermosetting epoxies, are preferred due to the ease with which an epoxy will bond to an anodized aluminum surface in accordance with preferred embodiments of the invention. Metallic solders, or
20 electrically conductive adhesives, electrically inter-connecting the metallic base 42 and a metallic cover 54 are preferred when the integrated circuit device 16 is to be shielded from electromagnetic interference.

25 The assembled ball grid array package 40 is bonded to bond pads 58 by the first electrically conductive means 50. Typically, the bond pads 58 are metallized pads inter-connected to circuitry on the system board 24. The first electrically
30 conductive means may be a low melting temperature solder such as a lead tin alloy.

Figures 3-9 illustrate in cross-sectional representation methods for forming electrically conductive vias in a metallic base. In Figure 3,
35 the metallic base 42 has a metallic core 60 with a

plurality of through holes 62. The through holes 62 may be formed by any conventional means. If the metallic core 60 is a metallic sheet, through holes 62 can be formed by a subtractive technique such as etching, punching, drilling or lasing. If the metallic core is formed by casting or sintering, the metallic core 60 can be formed with preexisting through holes 62. After the through holes 62 are formed, a dielectric layer 64 coats the surfaces of the metallic core 60, including the walls of the through holes 62. When the metallic core is aluminum, suitable methods for forming the dielectric layer 64 include anodization and chromating.

The dielectric layer has a thickness sufficient to prevent current leakage from conductive vias formed in the through holes to the metallic core 60. When the dielectric layer 64 is an anodization layer, a suitable thickness is from about 0.0076 millimeter to about 0.038 millimeter (0.0003-0.0015 inch).

When the metallic core 60 is copper or a copper based alloy, the dielectric layer 64 may be a refractory layer formed in situ, from the alloying constituents of the copper alloy. One suitable copper alloy for in situ formation of the dielectric layer is C638, nominal composition by weight 95% Cu, 2.8% Al, 1.8% Si, 0.4% Co, which on heating in an atmosphere containing a trace of water vapor forms an alumina surface layer. Alternatively, the copper alloy metallic core 60 may be coated with a material capable of forming a dielectric layer, such as vacuum deposited aluminum, which is then made electrically nonconductive by anodization or chromating.

The electrically conductive vias are formed by any suitable method. In Figure 4, a copper slug 66 having a length slightly longer than the through hole 62 is inserted in the hole and swaged to deform the pin head 68 and terminal end 70, mechanically locking the copper slug in the hole. The terminal end 70 terminates approximately at the exterior end 48 of the metallic substrate 42. A first electrically conductive means 50 is then bonded to the terminal end.

Any suitable means may be used to adhere the first electrically conductive means 50 to the terminal end 70. When the first electrically conductive means 50 is a solder foil, a tack weld may be used. A drop of liquid solder may be deposited on each terminal end 70. The liquid solder does not wet the dielectric layer 64 so precise location of the solder drop is not required. The molten solder will accumulate over the terminal pin. Applicants believe a solder dip may also be suitable. Solder paste can be deposited by any controlled alignment deposition means such as screen printing or dispensing from a syringe guided by a pattern recognition means. Other solder deposition means include plating onto the terminal pins as well as evaporation or sputtering through a mask.

When the first electrically conductive means 50 is a polymer adhesive or an electrically conductive glass, a partial cure, known in the art as tacking, may be utilized to adhere the components. Liquid polymers and glass pastes may be deposited by any controlled alignment means as described above.

A second method of forming the electrically conductive via is illustrated in Figure 5. A terminal pin 72 having a pin head 68 with a diameter

larger than the diameter of the through hole 62 is inserted through the through hole. The terminal end 70 of the terminal pin 72 terminates approximately at the exterior surface 48 of the metallic base 42.

5 A sufficiently large volume of first electrically conductive means 50 is bonded to the terminal end 70 of the terminal pin 72 such that the first electrically conductive means extends beyond the diameter of the through hole 62, thereby locking the

10 conductive via in place.

Figure 6 illustrates another method to form the conductive vias. The terminal pin 74 has a pin head 68 with a diameter larger than the diameter of the through hole 62. The terminal end 70 terminates

15 approximately at the exterior end 48 of the metallic substrate 42. The diameter 76 of the terminal pin 74 is significantly less than the diameter of the through hole 62, typically on the order of from about one third to about one half the diameter of

20 the through hole. The first electrically conductive means 50 is selected to be a fluid material such as molten solder or low viscosity polymer adhesive. Sufficient first electrically conductive means 50 is deposited within the through hole 62 to fully occupy

25 the area of the through hole and extend slightly beyond the exterior surface 48 of the metallic substrate 42.

The embodiment of Figure 6 as well as other embodiments including headed pins, is equally suited

30 for headless pins which are supported by an internal circuit board by any suitable means such as solder or a press fit.

Rather than utilize the first electrically conductive means to bond the electrically conductive

35 via in place, an embodiment as illustrated in Figure

7 may be utilized. The terminal pin 74 has a pin head 68 with a diameter larger than the diameter of the through hole 62. A dielectric sealing means 78, such as a polymer adhesive or sealing glass, bonds the shank of the terminal pin 74 to the walls of through hole 62 and provides additional electrical isolation between the electrically conductive via and the metallic substrate 42. One suitable sealing glass is disclosed in European Patent No. 90 400,134.4 to Electronique Serge Dassault and has the molar composition 20-50% sodium oxide, 5-30% barium oxide, 0.5-3% aluminum oxide, 40-60% phosphoric anhydride up to 7% aluminum nitride. This glass is disclosed to be suitable for bonding an anodized aluminum substrate to a nickel plated copper pin. A first electrically conductive means 50 is then bonded to the terminal end 70 as described above.

A coefficient of thermal expansion mismatch between a terminal pin and the metallic substrate may be utilized to form electrically conductive vias as illustrated in Figures 8A and 8B. In Figure 8A, a metallic core 60 is coated with a dielectric layer 64. A terminal pin 74 formed from a different metallic material is placed in through hole 62 and supported by pin head 68. The metallic core 60 and the composition of the terminal pin 74 are selected such that the coefficient of thermal expansion of the metallic core 60 is greater than that of the terminal pin 74. For example, the metallic core 60 can be aluminum or an aluminum based alloy and the terminal pin 74 can be copper or a copper base alloy. Both the metallic core and terminal pin are heated to a temperature sufficiently high to cause both materials to expand appreciably without thermal

degradation (such as precipitation hardening or annealing) of either component.

While hot, the terminal pin is inserted in the through hole. When the combination is cooled, the
5 higher coefficient of thermal expansion of the metallic substrate 60 causes the through hole 62 to collapse more than the diameter of the terminal pin 74, forming a tight press fit as illustrated in Figure 8B. A first electrically conductive means 50
10 is then bonded to the terminal end 70 of the press fit, terminal pin 74.

The conductive via need not be a rigid structure. In Figure 9, an electrically conductive paste 80 is utilized. The electrically conductive
15 paste 80 fills the through hole 62 and when cured, forms an electrically conductive via. Suitable electrically conductive pastes include a solder paste such as a lead tin alloy solder, such as 60% SN/40% Pb, or a silver filled epoxy resin.

Figure 10 illustrates in top planar view means for electrically interconnecting the internal end of the electrically conductive via 44 to an electronic device 16 mounted on the metallic base 44. This
20 second electrically conductive means may be by direct deposition of electrically conductive circuit traces on the dielectric layer or by inclusion of an internal circuit board. The internal circuit board may be flexible (for example, support on a thin
25 layer of polyimide), rigid (for example, supported by an FR-4 epoxy) or semi-rigid. Figure 10
30 illustrates direct deposition methods. An electrically conductive thick film paste 82 may be screened on the dielectric layer and extend from the electrically conductive via to wire bond pads 84 in
35 the vicinity of the integrated circuit device. Wire

bonds 18 then complete the second electrically conductive means. One suitable thick film paste is silver powder suspended in an organic binder.

5 A thin film may be deposited on the dielectric layers by evaporation or sputtering. The thin films may include layers of chromium and copper. Unlike the thick film paste 82 which is deposited subsequent to forming an electrically conductive via, the thin film is generally deposited prior to
10 formation of the electrically conductive via 44.

Alternatively, a portion of an internal circuit board 88, known in the art as an interposer circuit, may be utilized. The interposer circuit 88 includes a dielectric layer 90, typically a polyimide, BT
15 resin or FR4 epoxy, which is glued to the dielectric layer of the metallic base 42. Copper foil circuit traces 92 are formed on the dielectric layer 90 either by electroless deposition followed by electroplating or by subtractive etching of an
20 adhesively bonded copper foil. The second electrically conductive means then includes either first and second wire bonds 18' or a combination of a copper foil 94, such as used in tape automated bonding (TAB), and wire bond 18. Either the bond
25 wire or the TAB foil may be directly bonded to a pin head 68 by thermocompression bonding or soldering.

Figure 11 illustrates in cross-sectional representation an internal circuit board 96 for electrical interconnection within the ball grid
30 array package. The internal circuit board 96 has a dielectric layer 98 which may be a rigid material such as a glass filled epoxy or a semi rigid or flexible material such as a polyimide. Electrically conductive vias 100 are formed through the
35 dielectric layer 98 such as by electroless

deposition of a thin layer of palladium followed by electrolytic deposition of copper. Alternatively, a thin dispersion carbon black may be deposited on the walls of through holes and a copper layer deposited on the carbon black dispersion by electrolytic or electroless means as disclosed in U.S. Patent No. 5,065,228 to Foster et al. Circuit pattern 102 is formed on a first side of the dielectric layer 98 contacting electrically conductive vias 100. The opposing side of the electrically conductive vias 100 is joined to the electrically conductive vias 44 by means of an electrically conductive joint 104 which may be a solder or electrically conductive polymer or glass adhesive.

Figure 12 illustrates in cross-sectional representation an internal circuit board 96 which does not require electrically conductive vias to interconnect the electrically conductive vias 44 to circuit traces 102. Nonconductive vias 106 are formed in the dielectric layer 98. The nonconductive vias 106 have a diameter larger than the pin head 68 of the electrically conductive vias 44. The pin heads extend within the nonconductive vias and are overlayed by circuit traces 102 and an electrically conductive joint 104 electrically bonds the pin head 68 to the circuit trace 102. The electrically conductive joint 104 may be a solder, conductive adhesive, or a direct thermocompression bond between the circuit traces 102 and the pin heads 68.

As illustrated in Figure 13, the terminal pin 74 may extend through both the self supporting circuit 96 and the metallic base 42. The pin head 68 is electrically inter-connected to a circuit trace 102 such as by soldering. The internal circuit board 96

-16-

is then bonded to the metallic substrate 42 by a dielectric such as an epoxy glue 108.

In Figure 14, the conductive vias are formed by an electrically conductive paste 80. The
5 electrically conductive paste 80 fills a nonconductive via formed through both a metallic base 42 and the internal circuit board 96. A dielectric sealant 108 bonds the dielectric layer 98 of the internal circuit board 96 to the metallic
10 base 42.

In addition to the improved thermal dissipation achieved through the use of a metallic substrate, Figure 15 illustrates another benefit of the metallic core 60. The dielectric layer 64 is
15 removed from select through holes 62'. The dielectric layer free through holes 62' may be formed by mechanically abrading the dielectric layer after formation, such as redrilling the through holes to a slightly larger diameter, or by masking
20 to prevent contact the with anodization or chromating solution. One of the conductive vias 110 is then electrically interconnected to a system board circuit trace 112 which is connected to a ground or power circuit. The entire metallic core
25 60 is then at the same voltage potential as the ground or power circuit 112. Each conductive via 110' which is electrically interconnected to the metallic core 60 is at the same voltage potential providing power or ground to the integrated circuit
30 device 16. Secondary ground or power plane vias 110' need not contact a system board circuit trace and may be underlied with a thermally conductive grease 114 to improve thermal dissipation from the integrated circuit device 16 to the system board 24.

-17-

In addition to the cavity up ball grid array package illustrated in Figure 2, a cavity down ball grid array package 120, illustrated in Figures 16 and 17, is also within the scope of the invention.

5 The cavity down package 120 is similar to the cavity up package described above, except the electrically conductive vias 44 extend through the cover 54 of the package.

10 The package base 122, defined as that surface to which the integrated circuit device 16 is adhered, may be formed from any thermally conductive metallic material. Fins 124 may be formed in the base 122 to enhance thermal dissipation. The electrically conductive vias 44 are bonded to circuitry 126
15 formed on the interior surface 46 of the base component and electrically interconnected to the integrated circuit. The cover component 54 may be formed from any suitable material such as a polymer, ceramic or metal. While it is desirable that the
20 coefficient of thermal expansion of the cover 54 approximately matched that of the base 122, in a preferred embodiment, the cover 54 is formed from a nonconductive material to eliminate the need to coat the walls of the through holes 62 with a dielectric
25 layer. The bond 56 between the base 122 and cover 54 may be any suitable material as described above.

Alternatively, as illustrated in Figure 17, the cover 54' may be a molding resin such as a thermosetting epoxy which is molded about the
30 electrically conductive vias 44, circuit traces 102 and integrated circuit device 16. Rather than wire bonding, in any configuration of ball grid array packages described above, the integrated circuit device 16 may be electrically interconnected
35 directly to circuit traces 102 by solder bumps,

-18-

typically referred to as flip chip bonding or C-4 bonding. Other conductive means for flip chip bonding such as conductive adhesives are also applicable.

5 While the ball grid array packages of the invention have been described in terms of metallic package components, the package designs are suitable for metallic composites and metallic compounds. Suitable metallic composites include
10 copper-tungsten, copper-silicon carbide and aluminum silicon carbide. The metallic composites are manufactured by any means known in the art such as sintering or infiltration. One suitable metallic
15 compound is aluminum nitride. An advantage of the metallic composites and metallic compounds is that the physical characteristics of the material may be specifically designed, for example, to eliminate a
coefficient of thermal mismatch between the package and a printed circuit board.

20 In addition to the metals, metallic composites, and metallic compounds described above, other ball grid array substrates such as epoxy glass, polyimides and ceramics may be utilized in combination with the conductive vias described
25 above.

 While the ball grid array packages of the invention have been described in terms of encapsulating a single integrated circuit device, the invention is equally applicable to multi-chip
30 packages and hybrid packages including a printed circuit board with a plurality of electronic devices bonded therein.

 It is apparent that there has been provided in accordance with this invention a ball grid array
35 package which fully satisfies the objects, means and

advantages set forth hereinbefore. While the invention has been described in combination with specific embodiments thereof, it is evident that many alternatives, modifications and variations
5 would be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

IN THE CLAIMS

1. An electronic package (40), characterized by:

5 a base (42) having interior (46) and exterior (48) surfaces;

a plurality of electrically conductive vias (44) extending through said base (42) and terminating approxi-mately at said exterior surface (48), said electrically conductive vias (44) adapted to receive
10 a first electrically conductive means (50) adjacent to said exterior surface (48);

a second electrically conductive means (52) inter-connecting said electrically conductive vias (44) to an electronic device (16) mounted on said
15 base (42); and

a cover (54) bonded (56) to said base (42) with said electronic device (16) disposed thereinbetween.

2. The electronic package (40) of claim 1 characterized in that said base (42) is selected
20 from the group consisting of metals, metal alloy, metallic composites and metallic compounds.

3. The electronic package (40) of claim 2 characterized in that said base (42) is an aluminum based alloy (60) at least partially coated with an
25 anodization layer (64).

4. The electronic package (40) of claim 2 characterized in that said base (42) is a copper based alloy (60) at least partially coated with a refractory oxide layer.

-21-

5 5. The electronic package (40) of claim 3 characterized in that said base (42) includes a plurality of through holes (62) and said electrically conductive vias (44) are metallic pins (72, 74) extending through said through holes (62).

6. The electronic package (40) of claim 5 characterized in that said anodization layer (62) coats the walls of at least some of said through holes (62).

10 7. The electronic package (40) of claim 6 characterized in that both ends (68, 70) of said metallic pin (72, 74) have a diameter larger than the diameter of said through hole (62).

15 8. The electronic package (40) of claim 6 characterized in that one end (68) of said metallic pin (72, 74) has a diameter larger than the diameter of said through hole (62) and the other end (70) of said metallic pin (72, 74) is coated with said first electrically conductive means (50).

20 9. The electronic package (40) of claim 8 characterized in that said first electrically conductive means (50) has a diameter larger than said through hole (62).

25 10. The electronic package (40) of claim 6 characterized in that said first electrically conductive means (50) extends within said through hole (62).

-22-

11. The electronic package (40) of claim 6 characterized in that a dielectric sealant (78) bonds the shank of said metallic pin (74) to said through hole (62).

5 12. The electronic package (40) of claim 3 characterized in that said base (42) includes a plurality of through holes (62) and said electrically conductive vias (44) are a conductive paste (80) extending through said through holes
10 (62).

13. The electronic package (40) of any one of claims 5, 6, 7, 8, 10, 11, and 12 characterized in that said first electrically conductive means (50) is selected from the group consisting of solders,
15 conductive polymers and conductive sealing glasses.

14. The electronic package (40) of claim 13 characterized in that said second electrically conductive means (52) is one or more means selected from the group consisting of thick films, thin
20 films, internal circuit boards, wire bonds and metallic foils.

15. The electronic package (40) of claim 6 characterized in that some of said metallic pins (72, 74) are electrically interconnected to said
25 metallic base (42).

16. An electronic package (120), characterized by:

a base (122) having a dielectric layer coating at least a portion thereof;

5 a cover (54, 54') having interior and exterior surfaces;

a plurality of metallic terminal pins (44) extending through said cover (54, 54') and terminating approximately at said exterior surface;

10 a means (102) for electrically interconnecting said metallic terminal pins (44) to an electronic device (16) mounted on said metallic base (122); and

a means (56) to bond said cover (54, 54') to said metallic base (122).

15 17. The electronic package (120) of claim 16 characterized in that said cover (54) is metallic and contains a plurality of through holes (62) for receiving said metallic terminal pins (44), at least a portion of the walls of said through hole (62)
20 coated with a dielectric layer.

18. The electronic package (120) of claim 17 characterized in that both said base (122) and said cover (54) are formed from an aluminum alloy and said dielectric layer is anodized aluminum.

25 19. The electronic package (120) of claim 18 characterized in that said means (102) for electrically interconnecting is one or more means selected from the group consisting of thick films, thin films, internal circuit boards, wire bonds and
30 metallic foils.

20. The electronic package (120) of claim 16 characterized in that said cover (54') is a polymer resin molded about said terminal pins (44).

21. A method for the manufacture of an
5 electronic package (40), characterized by:
forming a plurality of through holes (62) in a
base (42);
inserting electrically conductive vias (44) into
said through holes (62);
10 electrically interconnecting (52) a
semiconductor device (16) to said electrically
conductive vias (44); and
bonding (56) a cover (54) to said base (42) with
said semiconductor device (16) disposed
15 therebetween.

22. The method of claim 21 characterized by the
further steps of:
selecting said base (42) to be a metal (60); and
coating at least a portion of said base (60) and
20 said through holes (62) with a dielectric layer
(64).

23. The method of claim 21 characterized in
that said electrically conductive vias (44) are
formed by inserting metallic pins (72, 74) into said
25 through holes (62) and essentially immobilizing said
metallic pins (72, 74) therein.

24. The method of claim 23 characterized in
that said immobilizing step comprises increasing the
diameter of both ends (68, 70) of said metallic
30 terminal pin (72, 74) to greater than the diameter
of said through hole (62).

-25-

25. The method of claim 23 characterized in that said immobilizing step comprises depositing a first electrically conductive material (50) on said end (70) of said terminal pin (72,74), said
5 electrically conductive material (50) having a diameter larger than the diameter of said through hole (62).

26. The method of claim 22 characterized in that said immobilizing step comprises depositing a
10 first electrically conductive material (80) within said through hole (62).

27. The method of claim 23 characterized in that said immobilizing step comprises depositing a dielectric (78) selected from the group consisting
15 of polymers and sealing glasses within said through hole (62).

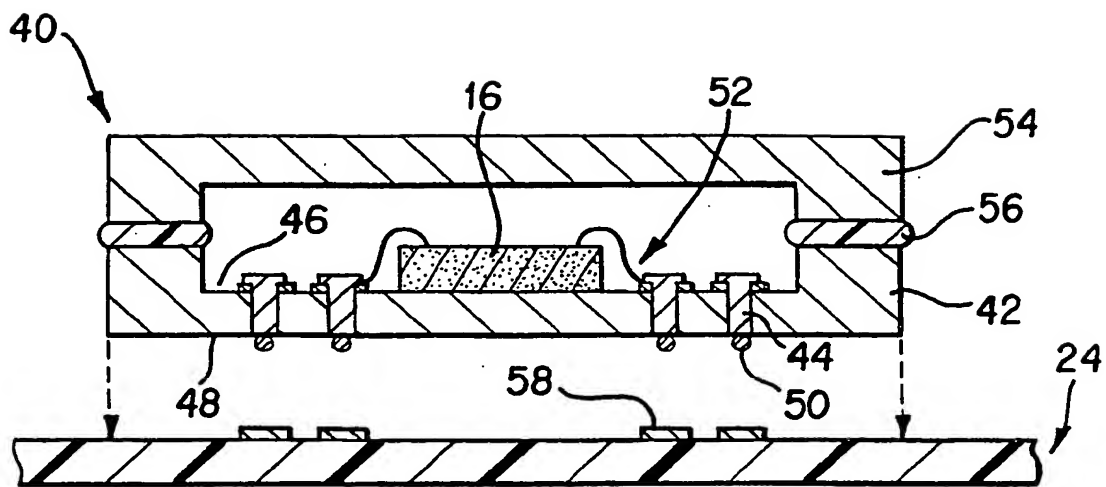
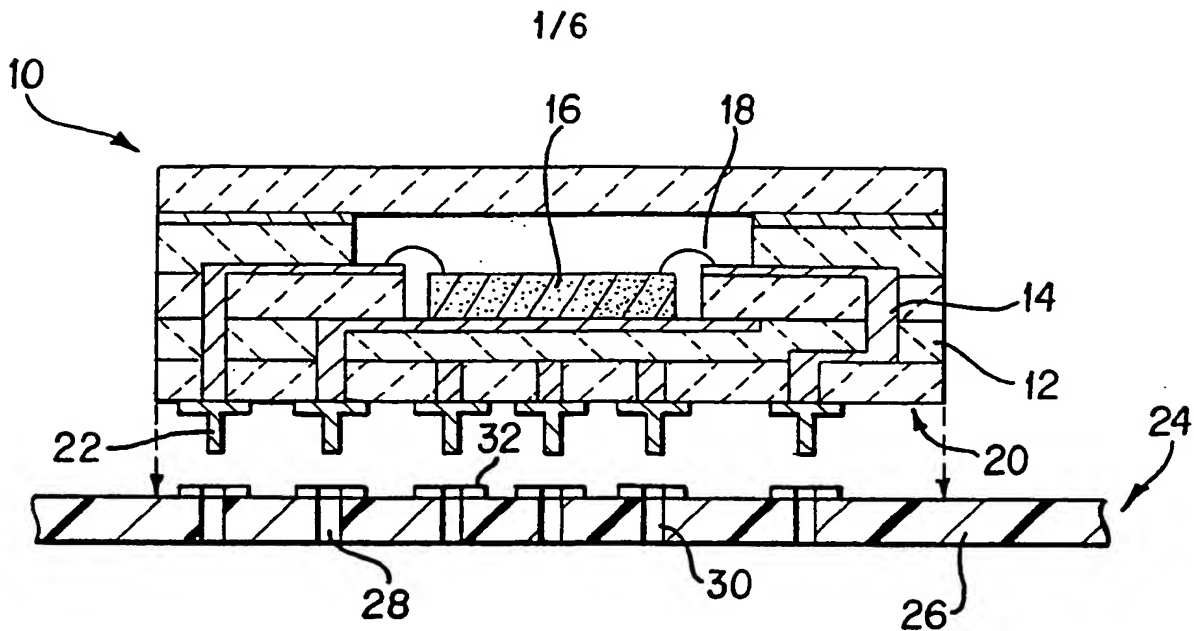
28. The method of claim 23 characterized in that said immobilizing step comprises:
selecting said metallic base (60) to have a
20 coefficient of thermal expansion greater than the coefficient of thermal expansion of said metallic pin (74); and

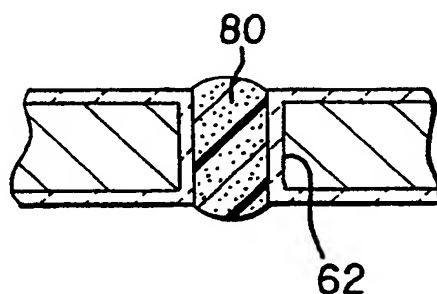
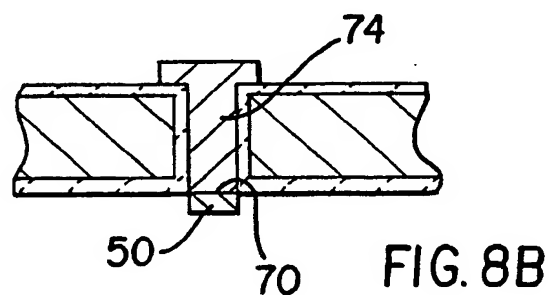
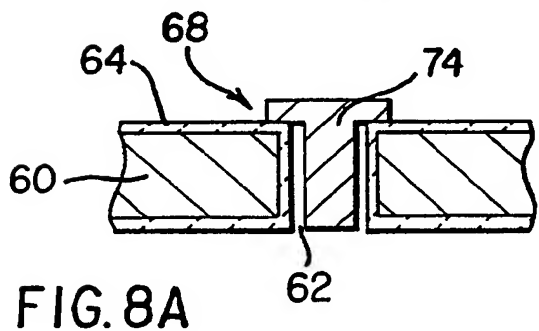
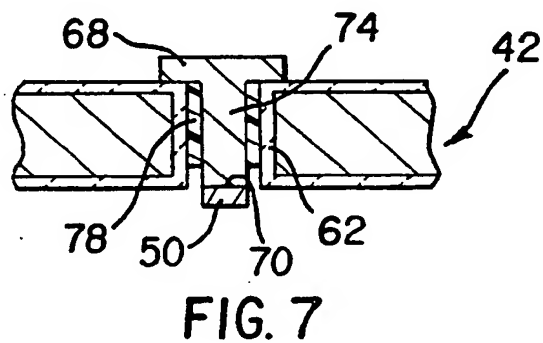
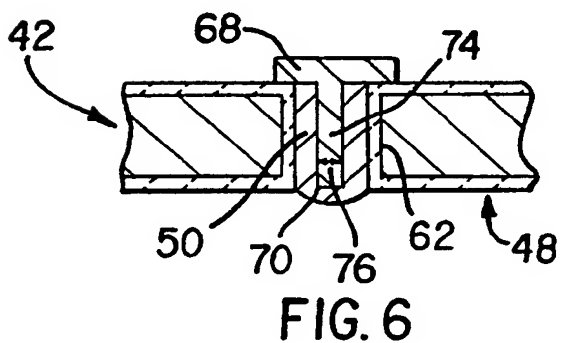
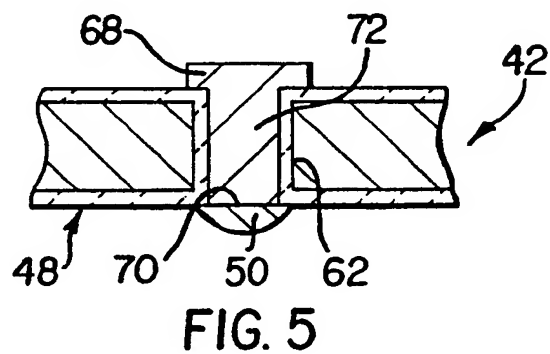
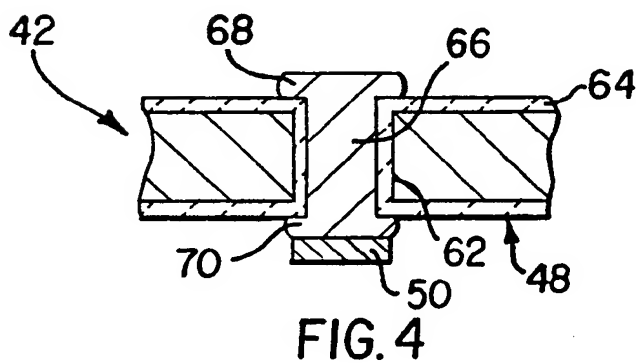
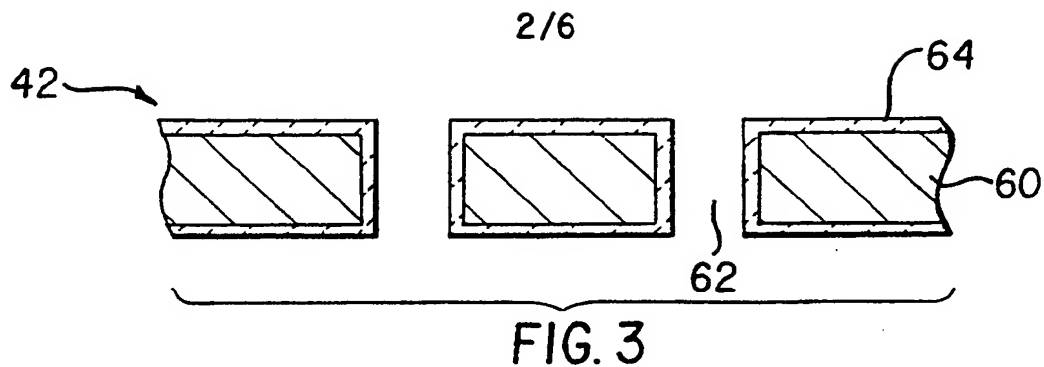
heating both said metallic base (60) and said metallic pin (74) to a temperature at which the
25 diameter of said through holes (62) is slightly larger than the diameter (76) of said metallic pin (74);

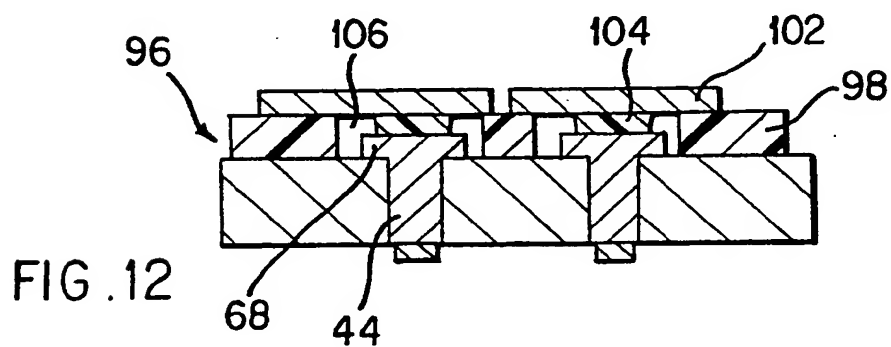
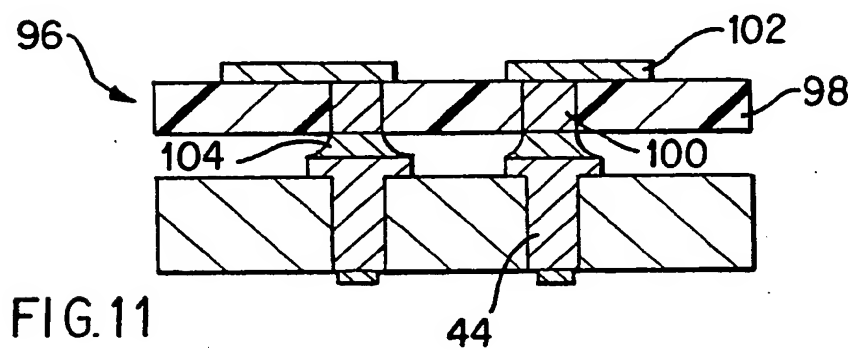
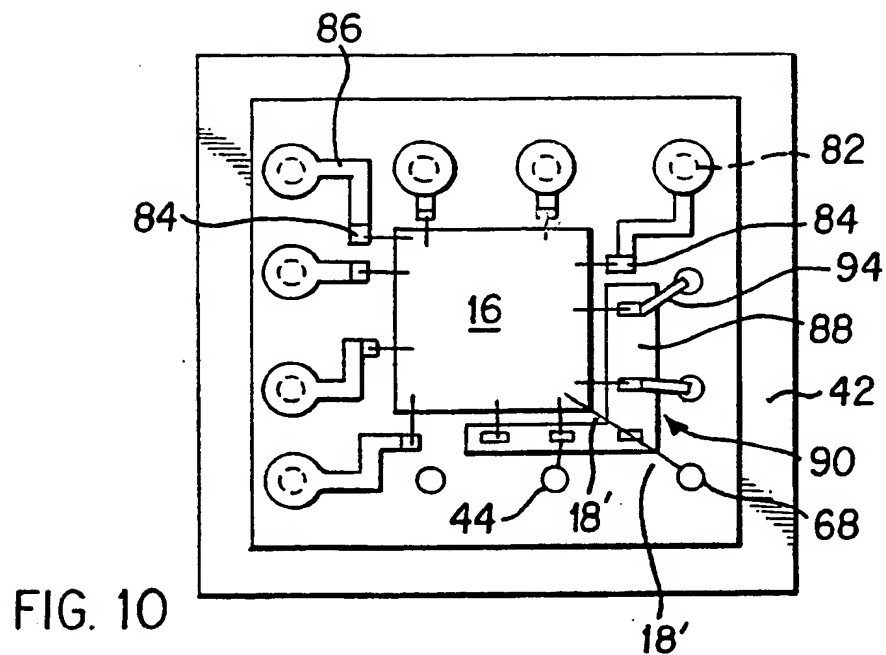
inserting said metallic pin (74) into said through hole (62); and
30 cooling said metallic base (60) and metallic pin (74).

29. The method of claim 22 characterized by the further step of removing said dielectric layer (64) from selected of said through holes (62).

30. The method of claim 22 characterized in
5 that selected of said through holes (110) are masked prior to said dielectric (64) coating step.







4/6

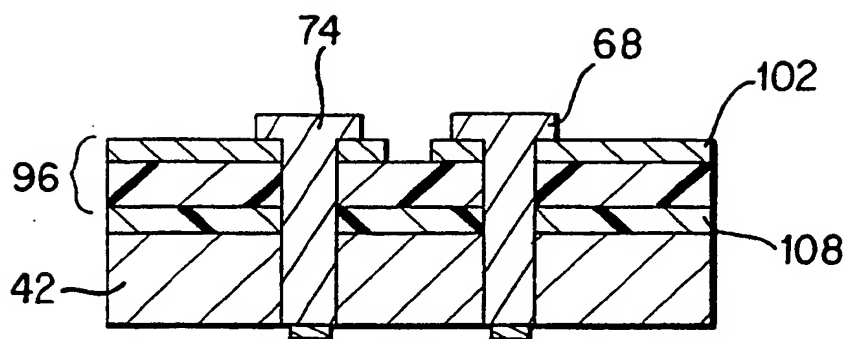


FIG. 13

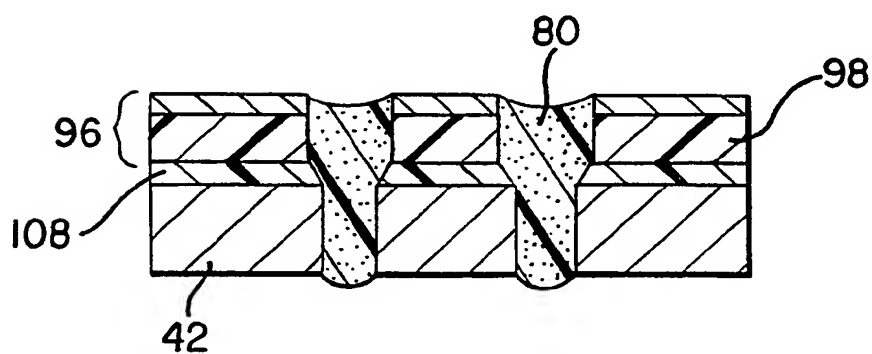


FIG. 14

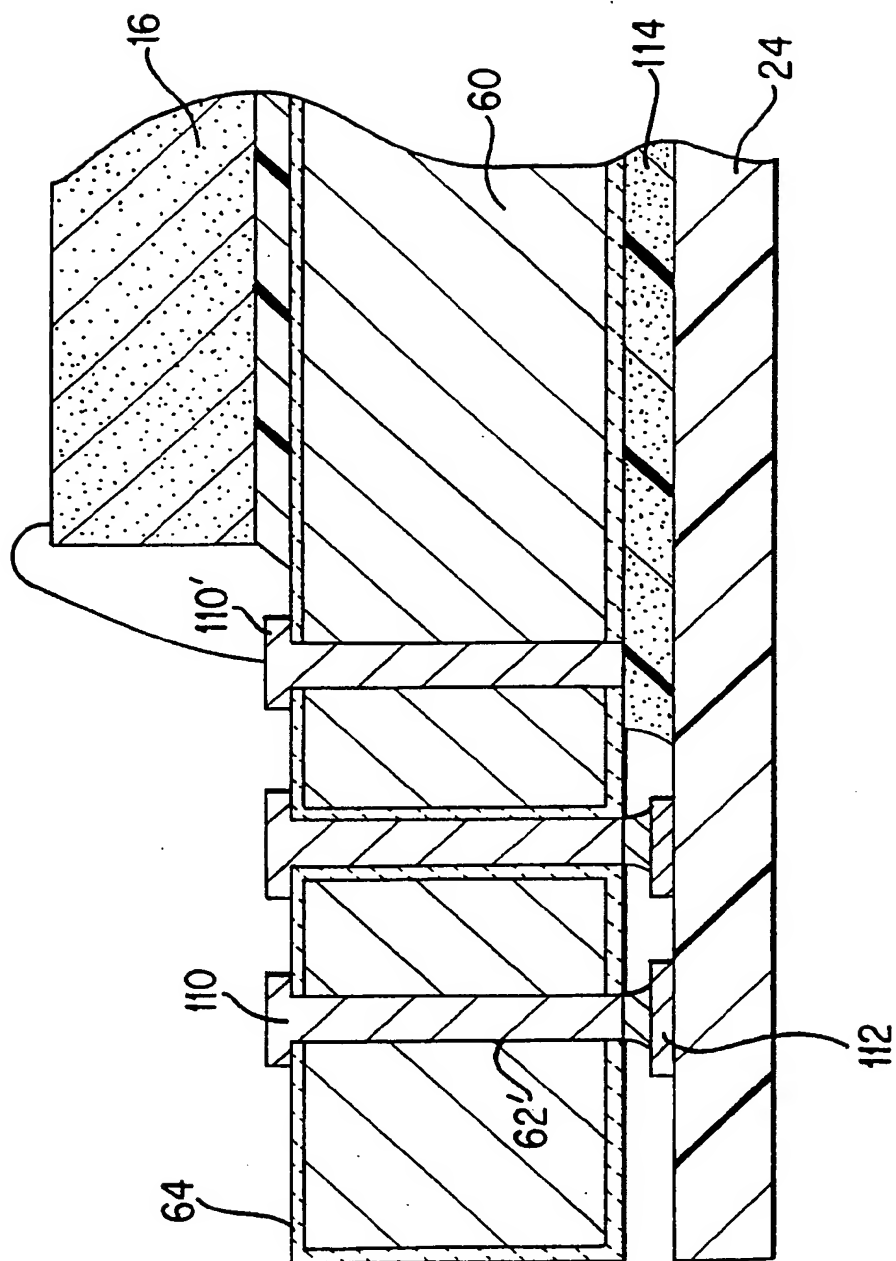


FIG. 15

6/6

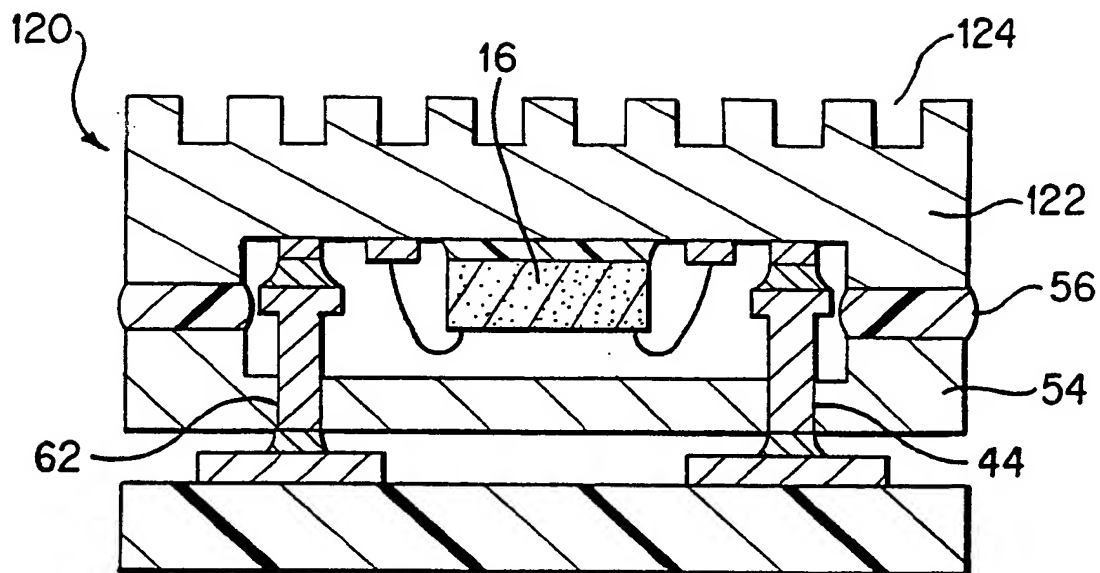


FIG. 16

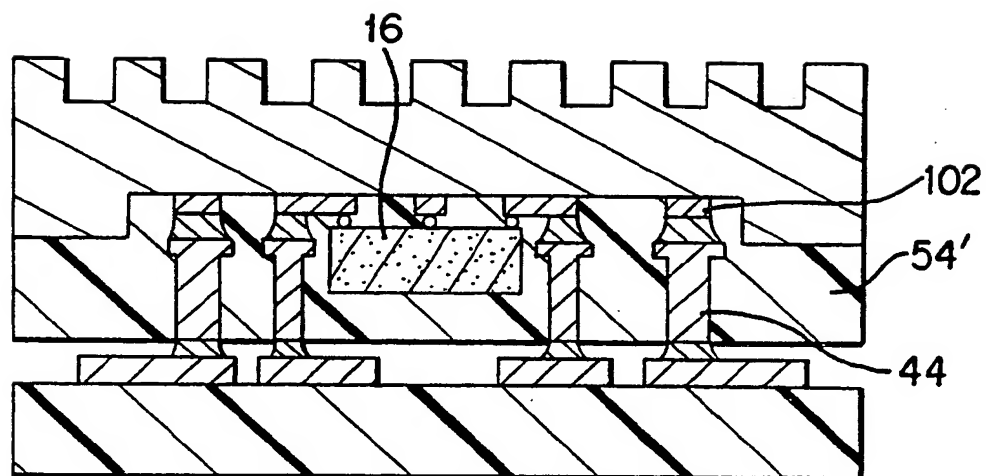


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/02113

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : IPC(5): HO1L 23/02,23/12

US CL : USCL: 257/693,697,698,706,707,708,779; 437/221,222,223,224

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : USCL: 257/693,697,698,706,707,708,779; 437/221,222,223,224

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A 2,905,873 (OLLENDORF ET AL) 22 SEPTEMBER 1959, SEE ENTIRE DOCUMENT	1-20
A	JP,A, 61-224344 (YAMAZOE) 06 OCTOBER 1986, SEE ENTIRE DOCUMENT	1-20
A	JP,A, 1-214052 (TAGUCHI) 28 AUGUST 1989, SEE ENTIRE DOCUMENT	1-20
A	EP,A, O 272,390 (SHINDO) 29 JUNE 1988, SEE ENTIRE DOCUMENT	1-20
A	US,A, 5,098,864 (MAHLIKAR) 24 MARCH 1992, SEE ENTIRE DOCUMENT	21-30

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be part of particular relevance	*X*	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Z*	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

16 MAY 1994

Date of mailing of the international search report

19 MAY 1994

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. NOT APPLICABLE

Authorized officer

for SHEILA CLARK

Telephone No. (703) 308-4924

BEST AVAILABLE COPY

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

Int. l. application No.
PCT/US94/02113

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 3,745,422 (CARNES) 10 JULY 1973, SEE ENTIRE DOCUMENT	21-30

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

BEST AVAILABLE COPY